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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,261	02/25/2002	Joon-Hoo Choi	8071-12 (OPP 011059US)	7814

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EXAMINER

WANG, GEORGE Y

ART UNIT	PAPER NUMBER
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2871

DATE MAILED: 03/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/083,261

Applicant(s)

CHOI ET AL.

Examiner

George Y. Wang

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) 3-19 and 24-32 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 2 and 6-12 is/are rejected.
- 7) ☒ Claim(s) 7-8 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 3-5, 13-19, 21, and 24-32 were withdrawn from further consideration pursuant to 37 CFR 1.142(b), there being no allowable generic or linking claim in Response filed 11 September 2003.

2. Claims 20, 22, and 23 are now withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected Specie (2), there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Response filed December 31, 2003.

Applicant agrees that Specie (1), Claims 1-2 and 6-12 are distinct from Specie (2), Claims 20 and 22-23 as set forth by Examiner. However, Applicant argues that the examination of the two species will not present an undue burden. Examiner disagrees and asserts that examination of both species will present an undue burden. Therefore, restriction is proper and final.

Claim Objections

3. Claims 7 and 8 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Claim 7 and 8 depend on Claim 6, but Claim 6 has the limitation "a-Si:C:O layer **or** a-Si:O:F layer." Thus, Claim 7, which depends only on the a-Si:C:O layer, and Claim 8, which

only depends on the a-Si:C:O layer, are improper because there is insufficient antecedent basis for this limitation in the claim since Claim 6 does not specify which layer. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 9, and 11-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Gu et al. (U.S. Patent No. 5,920,084, hereinafter "Gu").

6. As to claim 1, Gu discloses a thin film transistor array substrate comprising an insulating substrate (fig. 6, ref. 9), a first signal line (fig. 6, ref. 17) formed on the insulating substrate, a first insulating layer formed on the first signal line (fig. 6, ref. 21), a second signal line formed on the first insulating layer while crossing over the first signal line (fig. 6, ref. 13, 15), a thin film transistor (TFT) connected to the first and second signal lines (fig. 6, ref. 23), a second insulating layer formed on the TFT with a first contact hole (fig. 27) exposing predetermined electrode of the TFT and having a dielectric constant about 4.0 or less (abstract; col. 7, line 65 – col. 8, line 18), and a first

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pixel electrode (fig. 6, ref. 3) formed on the second insulating layer while being connected to the predetermined electrode of the TFT through the first contact hole (fig. 6, ref. 35; col. 10, line 66 – col. 11, line 5).

7. As per claim 9, Gu discloses a TFT array substrate as recited above where the second insulating layer has a dielectric constant of about 2 to about 4 (abstract; col. 7, line 65 – col. 8, line 18).

8. Regarding claims 11-12, Gu discloses a TFT array substrate as recited above where the pixel electrode is made of an optically transparent and electrically conductive material such as ITO (col. 8, lines 21-22).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

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not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 2 and 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gu in view of Chen et al. (U.S. Patent No. 6,362,028, hereinafter "Chen").

11. As per claim 2, Gu discloses a TFT array substrate with a first insulating layer made of silicon nitride (col. 9, lines 58-64) and other materials with dielectric of 4 or less (col. 7, line 65 – col. 8, line 18) as recited above, however, the reference fails to specifically disclose a second bottom dielectric layer.

Chen discloses a TFT substrate having a first insulating layer with a top layer (fig. 1, ref. 20) made of silicon nitride and a bottom layer (fig. 1, ref. 16) made of a low dielectric material.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a first insulating layer with a top layer formed of silicon nitride and a second bottom layer formed of a dielectric of 4 or less since one would be motivated to reduce defects such as pin holes and to improve yield (col. 2, lines 25-28).

12. Regarding claim 6, Gu discloses a TFT array substrate (abstract) as recited above with a second insulating layer formed with an a-Si layer, however, the reference

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fails to specifically disclose a second insulating layer formed with an a-Si:C:O or a-Si:O:F layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed a second insulating layer formed with an a-Si:C:O or a-Si:O:F layer since one would be motivated to use these well known amorphous silicon materials to improve contact resistance and to reduce chemical contaminants, which ultimately shields the TFT from plasma damage and residual photoresists resulting in a TFT array substrate of improved reliability (Chen, abstract).

13. As to claims 7-8, Gu discloses an a-Si TFT array substrate as recited above (abstract), however, the reference fails to specifically the a-Si layer being formed by a PECVD method. Nevertheless, even though the product-by-process limitation “is formed through plasma enhanced chemical vapor deposition (PECVD)...” is recognized as limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior art product was made by a different process. *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985). See also MPEP 2113.

14. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gu in view of Sasano et al. (U.S. Patent No. 5,671,027, hereinafter “Sasano”).

Gu discloses a TFT array substrate as recited above where the first signal line is formed of alloys of Cr or Al (col. 10, lines 5-8).

However, the reference fails to specifically disclose that the first signal line includes a first and a second layer.

Sasano discloses a TFT substrate with a first signal line having a first layer (fig. 2a, ref. g1) made of Cr alloy (col. 13, lines 5-6) and a second layer (fig. 2a, ref. g2) made of Al alloy (col. 13, lines 18-19).

It would have been obvious to one of ordinary skill at the time the invention was made to have a first signal line having a first layer made of Cr alloy and a second layer made of Al alloy since one would be motivated to reduce short circuiting that leads to defects and deterioration (col. 1, lines 65-68) and to increase excellent display performance (col. 2, lines 16-18).

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to George Y. Wang whose telephone number is 571-272-2304. The examiner can normally be reached on M-F, 8 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gw
March 10, 2004


ROBERT H. KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 28